side wall and a surface of the chip opposite the surface where the electrodes are located have been grinded or polished to a common level .

2. (Amended) The [chip-like] electronic chip component according to claim 1 wherein said protective material comprises either one of an organic insulating resin and an organic insulating material.

3. (Amended) The [chip-like] electronic chip component according to claim 1, comprising a semiconductor chip diced at a position of said protective material for mounting on a packaging substrate, wherein [said electrode is formed on a device surface, and a whole area] all of said side wall [thereof] is covered with said protective material.

4. (Amended) The [chip-like] electronic chip component according to claim 3, wherein a solder bump is formed on [said electrode] each of said electrodes.

5. (Amended) The [chip-like] electronic chip component according to claim 1, wherein a plurality of [a same or] different types of semiconductor chips are bonded and integrated by said protective material.

6. (Amended) A pseudo wafer comprising a plurality of [a] same or different [types of chip-like] electronic chip components each having [at least] all [their] electrodes formed on one surface thereof, bonded [with] to each other with a protective material coated on side walls therebetween, and [another surface opposing said one surface being fabricated to reduce a

thickness thereof] wherein there is no protective material located on the one surface of the chip where all the electrodes are formed and further wherein the protective material on the side wall and a surface of the chip opposite the surface where the electrodes are located have been grinded or polished to a common level ..

8. (Amended) The pseudo wafer according to claim 6, wherein said pseudo wafer is diced into a single semiconductor chip [or into a unit of semiconductor chips integrating a plurality of a same or different types of semiconductor chips] at a position of said protective material [therebetween] for mounting on a packaging substrate.

9. (Amended) The pseudo wafer according to claim 8, wherein a solder bump is formed on [said electrode] each of said electrodes.

## REMARKS

Applicant thanks the Examiner for acknowledging receipt of Applicant's foreign priority documents that have been submitted pursuant to 35 U.S.C. §119. In accordance with the Examiner's request, Applicant has attached a proposed Drawing Amendment which proposes modification of Figures 9-12E to include the designation "Prior Art." Applicant requests entry of these proposed drawing changes.

In regard to paragraph 4 of the Examiner's Office Action, Applicant agrees that the phrase "at least its all electrodes" should probably be modified to "all electrodes." However, there is no indication as to where the reference phrase is found in the Specification. Applicant has made the appropriate corresponding changes to the claims. Accordingly,